WHAT IS CLAIMED IS:

1. A reference voltage generation circuit, comprising:

at least one reference cell having a source electrode and a drain electrode;

a plurality of first sense circuits connected to the reference cell and including an N-channel transistor, a P-channel transistor, a plurality of input ends and a plurality of output ends; and

a plurality of second sense circuits each for receiving an output from a corresponding one of the plurality of first sense circuits, the plurality of second sense circuits each having a load circuit, an N-channel transistor, a plurality of input ends and a plurality of output ends.

2. A reference voltage generation circuit according to claim 1, wherein the plurality of first sense circuits each generate a first duplicate voltage based on a voltage from the reference cell, and the plurality of second sens circuits each generate a second duplicate voltage based on the first duplicate voltage.

3. A memory reading circuit for a semiconductor memory

device, comprising:

a reference voltage generation circuit according to claim 2;

a third sense circuit connected to a selected memory cell and having an N-channel transistor, a P-channel transistor, a plurality of input ends and a plurality of output ends; and

a fourth sense circuit for receiving an output from the third sense circuit, the fourth sense circuit having a load circuit, an N-channel transistor, a plurality of input ends and a plurality of output ends,

wherein the information is read using an output from each of the plurality of second sense circuits and an output from the fourth sense circuit.

4. A memory reading circuit according to claim 3, for reading information from the selected memory cell by supplying a reference voltage to one of two input ends of a sense amplifier and supplying a voltage from th selected memory cell to the other of the two input ends, wherein an output from each of the plurality of second sense circuits and an output from the fourth sense circuit are input to the sense amplifier.

5. A memory reading circuit according to claim 4, wherein:

the load circuit of each of the plurality of second sense circuits of the reference voltage generation circuit is a P-channel transistor, and the load circuit of the fourth sense circuit is a P-channel transistor, and

a gate electrode and a drain electrode of one of the plurality of second sense circuits are connected to a gate electrode of the P-channel transistor of the fourth sense circuit, so that a load characteristic of the fourth sense circuit is equal to a load characteristic of the one of the plurality of second sense circuits.

6. A memory reading circuit according to claim 5, wherein the reference voltage generation circuit shortcircuits an output from the fourth sense circuit and an output from the one of the plurality of second sense circuits through a transistor, and the output from the fourth sense circuit and the output from the one of the plurality of second sense circuits are transferred to a respective prescribed potential from the same level after being released from the shortcircuiting.

7. A memory reading circuit according to claim 3, wherein an output from each of the plurality of second sense circuits

and an output from the fourth sense circuit are shorcircuitable, and the output from the fourth sense circuit is output through an inverter circuit.

8. A memory reading circuit according to claim 7, wherein:

the load circuit of each of the plurality of second sense circuits of the reference voltage generation circuit is a P-channel transistor, and the load circuit of the fourth sense circuit is a P-channel transistor, and

a gate electrode and a drain electrode of one of the plurality of second sense circuits are connected to a gate electrode of the P-channel transistor of the fourth sense circuit, so that a load characteristic of the fourth sense circuit is equal to a load characteristic of the one of the plurality of second sense circuits.

9. A memory reading circuit according to claim 8, wherein the reference voltage generation circuit shortcircuits an output from the fourth sense circuit and an output from the one of the plurality of second sense circuits through a transistor, and the output from the fourth sense circuit and the output from the one of the plurality of second sense circuits are transferred to a respective prescribed potential from the same level after being released from

the shortcircuiting.

10. A memory reading circuit for a semiconductor memory device, comprising:

a reference voltage generation circuit according to claim 1;

a third sense circuit connected to a selected memory cell and having an N-channel transistor, a P-channel transistor, a plurality of input ends and a plurality of output ends; and

a fourth sense circuit for receiving an output from the third sense circuit, the fourth sense circuit having a load circuit, an N-channel transistor, a plurality of input ends and a plurality of output ends,

wherein the information is read using an output from each of the plurality of second sense circuits and an output from the fourth sense circuit.

11. A memory reading circuit according to claim 10, for reading information from the selected memory cell by supplying a reference voltage to one of two input ends of a sense amplifier and supplying a voltage from th selected memory cell to the other of the two input ends, wherein an output from each of the plurality of second

sense circuits and an output from the fourth sense circuit are input to the sense amplifier.

12. A memory reading circuit according to claim 11, wherein:

the load circuit of each of the plurality of second sense circuits of the reference voltage generation circuit is a P-channel transistor, and the load circuit of the fourth sense circuit is a P-channel transistor, and

a gate electrode and a drain electrode of one of the plurality of second sense circuits are connected to a gate electrode of the P-channel transistor of the fourth sense circuit, so that a load characteristic of the fourth sense circuit is equal to a load characteristic of the one of the plurality of second sense circuits.

13. A memory reading circuit according to claim 12, wherein the reference voltage generation circuit shortcircuits an output from the fourth sense circuit and an output from the one of the plurality of second sense circuits through a transistor, and the output from the fourth sense circuit and the output from the one of the plurality of second sense circuits are transferred to a respective prescribed potential from the same level after being released from

the shortcircuiting.

14. A memory reading circuit according to claim 11, further comprising a load circuit for performing current-to-voltage conversion of the selected memory cell and the reference cell, the load circuit including at least one of a transistor and a resistor, wherein the load circuit is directly connected to a drain electrode of the selected memory cell and the drain electrode of the reference cell.

15. A memory reading circuit according to claim 10, wherein an output from each of the plurality of second sense circuits and an output from the fourth sense circuit are shorcircuitable, and the output from the fourth sense circuit is output through an inverter circuit.

16. A memory reading circuit according to claim 15, wherein:

the load circuit of each of the plurality of second sense circuits of the reference voltage generation circuit is a P-channel transistor, and the load circuit of the fourth sense circuit is a P-channel transistor, and

a gate electrode and a drain electrode of one of the plurality of second sense circuits are connected to

a gate electrode of the P-channel transistor of the fourth sense circuit, so that a load characteristic of the fourth sense circuit is equal to a load characteristic of the one of the plurality of second sense circuits.

17. A memory reading circuit according to claim 16, wherein the reference voltage generation circuit shortcircuits an output from the fourth sense circuit and an output from the one of the plurality of second sense circuits through a transistor, and the output from the fourth sense circuit and the output from the one of the plurality of second sense circuits are transferred to a respective prescribed potential from the same level after being released from the shortcircuiting.

18. A memory reading circuit according to claim 15, further comprising a load circuit for performing current-to-voltage conversion of the selected memory cell and the reference cell, the load circuit including at least one of a transistor and a resistor, wherein the load circuit is directly connected to a drain electrode of the selected memory cell and the drain electrode of the reference cell.

19. An electronic information device capable of reading

information using a memory reading circuit according to claim 10.

20. An electronic information device capable of reading information using a memory reading circuit according to claim 1.